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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/508,879 | 06/13/2005 | Alexander Krasin | SC11823TC | 1120 |

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| EXAMINER | |
|---|---|
| KITOV, ZEEV V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/508,879 | KRASIN, ALEXANDER | |
| | Examiner | Art Unit | |
| | Zeev Kitov | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1- 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

### *Objection*

Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim 1. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. As a matter of fact, Claim 6 does not recite any additional limitation.

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a) because they fail to show the voltage curves in identifiable manner, as described in the specification. Fig. 2 and 3 should be provided with identifying labels next to the curves. Any structural detail that is

essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 2 – 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. A reason for that is that the claims include following limitation: "PMOSFET (or NMOSFET, or both) capacitor has a non-linear characteristic". It is neither clear from the claim language, nor disclosed by Specification, what non-linear characteristic is assumed. Such characteristic presumably is a dependence of the transistor capacitance on a regime of the transistor. However, since no details or explanation is provided, the claims are considered indefinite. For purpose of examination it was assumed that the non-linearity is observed in the capacitance dependence on gate to substrate voltage.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar (US 5,287,241) in view of Segervall (US 6,667,870) and Ker et al. (US 6,912,109). Regarding Claims 1 and 6, Puar discloses following elements: the circuit being connected to a power rail and a ground rail (Vdd and Vss in Fig. 4) and to clamping transistor (P3 in Fig. 4), the circuit includes: a PMOSFET resistor with a gate connected to the ground rail (P4 in Fig. 4), a drain connected to the input node of the clamping transistor (P3 in Fig. 4), a source and a bulk connected to the power rail, an NMOSFET capacitor (C1 in Fig. 4) with a gate connected to the input node of the clamping

transistor (see Fig. 6), a drain, a source and a bulk connected to the ground rail. However, it does not disclose an additional capacitor and preamplifier. Segervall discloses the additional capacitor (C3 in Fig. 5) connected between the power rail and the input node of the clamping transistor (M2 in Fig. 5). Both references have the same problem solving area, namely providing ESD protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by adding the capacitor according to teachings of Segervall, because as Segervall states (col. 6, lines 18 – 26), the capacitor is necessary to reduce the turn on time of the clamp transistor.

However, Segervall does not disclose details of the capacitor connection and preamplifier. Ker et al. disclose the PMOSFET capacitor (48 in Fig. 12) with a gate connected to the inverter's (30, 28 in Fig. 12) input node, a bulk connected to the power rail (Vdd in Fig. 12). Both references have the same problem solving area, namely providing ESD protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Puar solution by implementing the capacitor in PMOSFET form and using the preamplifier according to teachings of Ker et al., because (I) the MOSFET implemented capacitor takes substantially smaller space in the integrated circuit than the metal capacitor and (II) due to use of the preamplifier, the clamp transistor is turned on earlier than it would be without the preamplifier.

As to the source and the drain connection, they are shorted to each other and left floating. The claim requires connection of the source and drain to the ground. As well

known in the art, the MOSFET transistor in addition to its gate-bulk capacitance has the drain-gate and the source-gate capacitances. Connecting the drain and source to the ground will add these capacitances in parallel to the power supply. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Puar solution by connecting the drain and source of the PMOSFET to the ground, because it would provide additional the power decoupling capacitors for the circuit.

Claims 2 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in view of Segervall, Ker et al. and Ho (US 5,731,739). As was stated above, Puar, Segervall and Ker et al. disclose all the elements of Claim 1. However, regarding Claims 2 – 4, they do not disclose the MOSFET capacitors having non-linear dependence on the gate-bulk voltage. As a matter of fact, these are pure functional limitations. Ho discloses that MOSFET capacitance is a non-linear function of the gate to substrate (bulk) potential difference (Fig. 3, col. 2, lines 26 – 43), i.e. non-linearity of the MOSFET capacitance is an inherent property of such capacitance.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in view of Segervall, Ker et al. and Statz et al. (US 5,825,601). As per Claim 5, it differs from Claim 1 rejected above by its limitation of the capacitance ratio changing when the voltage at the power rail exceeds NMOSFET threshold. Statz et al. disclose that both NMOS and PMOS capacitance increase their value when the voltage between the gate

and the substrate exceeds the threshold value (col. 3, lines 56 – 61, and col. 4, lines 47 – 51). Eventually, in the Puar circuit modified according to teachings of Segervall and Kerr, the capacitance of the NMOSFET will follow the rule. When the voltage at the power rail exceeds the threshold of the NMOS transistor its capacitance increases and the ratio of capacitance of the PMOSFET to the capacitance of the NMOSFET will decrease. The Statz et al. reference is recited only to demonstrate that the modified version of the Puar circuit will have inherent increase of capacitance.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K.
2/17/2006

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